45 GHz Highly Integrated Phase-Locked Loop Frequency Synthesizer in SiGe Bipolar Technology

Student paper

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Abstract **This paper presents a highly integrated 45 GHz phase-locked loop frequency synthesizer. The monolithic circuit consists of a voltage-controlled oscillator with frequency doubler and divide-by-16 static frequency divider and is manufactured in a pre-production low-cost 0.4 μm/85 GHz SiGe bipolar technology. The power consumption is 650 mW from the 5 V supply. External synthesizer building blocks are a commercially available PLL-IC, a passive loop filter, and a reference oscillator.**

I. Introduction

The demand for wireless services will increase rapidly within the next few years. Wireless local area networks (WLANs) at 2.4 GHz, 5.2 GHz, and 17.2 GHz, satellite communications systems at 8 GHz and 10 GHz, and radio links at 13, 15, and 18 GHz are examples for wireless systems up to 20 GHz. Above 20 GHz, point-to-multipoint systems between 24.5 and 29.5 GHz, local multipoint distribution systems (LMDS) at 28 and 38 GHz, and European microwave video distribution systems (MVDS) at 42 GHz are emerging. In all these wireless systems frequency synthesizers are needed.

For the mobile communications market with operating frequencies up to 2.5 GHz highly integrated circuits are available from many manufacturers. These dividers, dual-modulus prescalers, and PLL-ICs (consisting of programmable dividers and phase detectors) for frequency synthesis are mostly fabricated in low-cost technologies like silicon bipolar, CMOS or BiCMOS.

Key building blocks to achieve carrier frequencies beyond 20 GHz are the voltage-controlled oscillator, the frequency divider, and the frequency multiplier. In this paper we demonstrate for the first time the monolithic integration of these three RF key building blocks for operating frequencies beyond 40 GHz. By combining these three blocks with already existing designs of PLL-ICs (e.g. [1], etc.) completely integrated frequency synthesizers for frequencies beyond 40 GHz are feasible.

Fig. 1 shows the frequency synthesizer in phase-locked loop (PLL) architecture realized in this work. The voltage-controlled oscillator (VCO) operates at half of the desired output frequency. The frequency doubler raises the VCO frequency to the desired output frequency. The prescaler converts the VCO frequency into the much lower frequency range which can easily be handled by commercially available PLL-ICs mentioned above.

Highly integrated Si-based synthesizers with VCO, frequency divider and phase detector on chip achieve operating frequencies around 7 GHz [2]. The highest operating frequency for completely integrated synthesizers reported is 34 GHz [3] realized in III-V semiconductor technology.

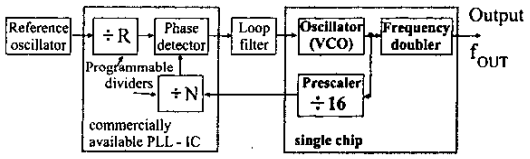

Fig. 1. Block diagram of frequency synthesizer in phase-locked-loop architecture

This work presents a monolithic IC consisting of a voltage-controlled oscillator with frequency doubler and divide-by-16 static frequency divider suitable for frequency synthesis for LMDS applications at 38 GHz and MVDS applications at 42 GHz. The circuit is fabricated in a low-cost 0.4 μm/85 GHz SiGe bipolar technology. External building blocks are only the commercially available PLL-IC, the passive loop filter, and the reference oscillator.

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To our knowledge the operating frequency of 45 GHz is the highest reported for highly-integrated frequency synthesizers up to date.

II. Circuit Design

Fig. 2 shows the block diagram of the monolithic VCO with frequency doubler and static frequency divider. All blocks are designed in fully differential logic. The two output buffers have balanced outputs, each of the buffers can drive a 50 Ω load.

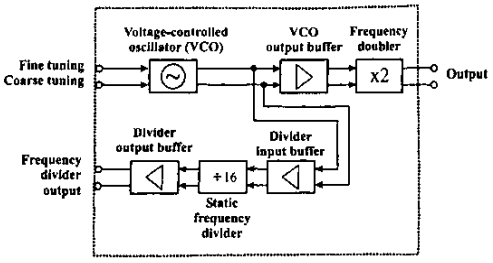

Fig. 2. Block diagram of the monolithic VCO with frequency doubler and static frequency divider

A. Voltage-Controlled Oscillator

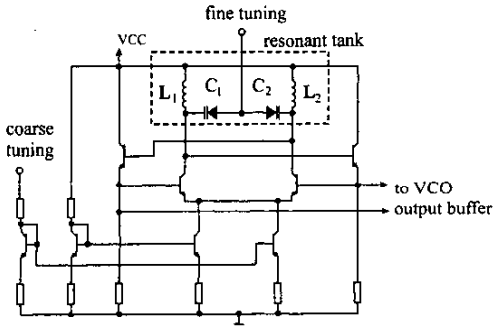

Fig. 3. Schematic of the voltage-controlled oscillator

Fig. 3 shows the VCO topology. The oscillator consists of a cross-coupled differential amplifier with a resonant LC circuit acting as load. Emitter followers in the feedback path help to reduce the loading of the resonant circuits by the input of the differential amplifier and achieve a high loaded Q of the resonator. On-chip spiral inductors and transistors used as varactors build the resonant circuits. A coarse tuning of the output frequency of the oscillator can be performed by varying the operating current of the oscillator [2].

B. Static Frequency Divider

The block diagram of the divide-by-16 static frequency divider is shown in fig. 4. The divider input buffer is realized with a differential amplifier and emitter followers for level shifting.

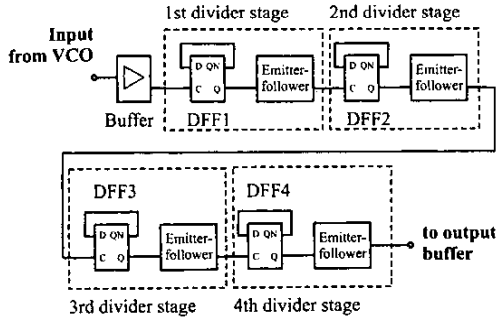

Fig. 4. Block diagram of the static divide-by-16 frequency divider

The static frequency divider consists of 4 D-type master-slave flip-flops (DFFs) and emitter followers for level shifting. The transistors of the first flip-flop operate at the current density for peak transit frequency. As the operating frequencies of the following flip-flops always decrease by the factor of two, their operating currents are reduced stage by stage to save power.
The divider output buffer is implemented as differential amplifier.

C. Frequency Doubler

Fig. 5 shows the schematic of the frequency doubler based on the Gilbert cell. The transistors of the three emitter followers and the Gilbert cell are optimized individually for the current densities for peak transit frequency. The frequency doubler has 50 Ω outputs.

D. Current Consumption

The simulated total current consumption of the monolithic VCO with frequency doubler and static frequency divider is 124 mA at the 5 V supply. The VCO with output buffer consumes 20 mA, the frequency doubler 31 mA, and the static divide-by-16 frequency divider with in- and output buffers 73 mA of the total supply current.

III. Technology

The circuit was fabricated in a pre-production 0.4 μm-SiGe bipolar technology [4] using a double-polysilicon self-aligned emitter-base configuration with effective emitter width of 0.2 μm. The transistors manufactured in this technology offer a maximum transit

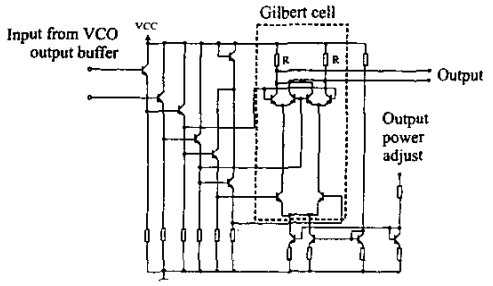

Fig. 5. Frequency doubler based on the Gilbert cell

frequency of 85 GHz, maximum oscillation frequency of 128 GHz, and CML gate delay time of 6.8 ps. The four available metallization layers enable low parasitic wiring capacitances. Fig. 6 shows the chip photograph of the monolithic VCO with frequency doubler and frequency divider.

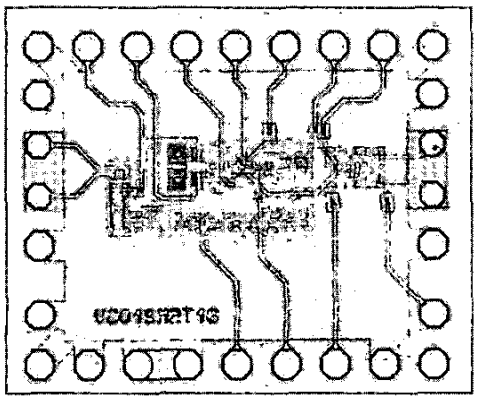

Fig. 6. Chip photograph (size: 860 μm x 700 μm)

IV. Experimental Results

All measurements were performed with wirebonded chips mounted on high-frequency ceramic substrates with thickness of 0.38 mm and supply voltage of 5 V. The low-frequency building blocks like the commercially available PLL-IC, the passive loop filter, and the reference oscillator were assembled on 0.31 mm high-frequency substrates (Fig. 7).

Fig. 8 shows the coarse tuning characteristic of the VCO with frequency doubler. The maximum output frequency is 45 GHz, the coarse tuning range is 10 GHz, and the fine tuning range is at least 4 GHz. The output power varies between -12 dBm and -16 dBm with de-embedding

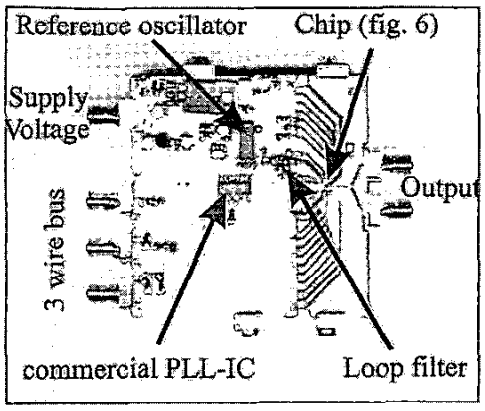

Fig. 7. Test fixture (size: 7 cm x 7 cm)

of the losses of the measurement equipment. The fundamental VCO signal at half of the output frequency is suppressed by 10 dB at 40 GHz output frequency.

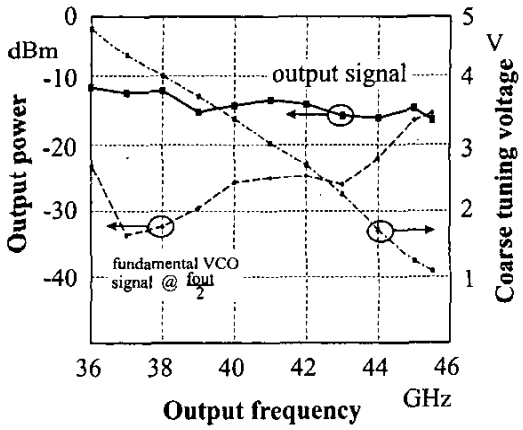

Fig. 8. Tuning characteristic of the VCO with frequency doubler and frequency divider

Fig. 9 shows the spectrum of the output signal in locked mode at 40 GHz without de-embedding of the losses of the measurement equipment. The free-running VCO with frequency doubler has a phase noise of -79.5 dBc/Hz at 1 MHz offset from the 40 GHz carrier.

A 3-pole passive structure was chosen to act as loop filter with a loop filter bandwidth of 16 kHz and a damping factor ξ of 0.85. The settling time for an output frequency step from 38 GHz to 40 GHz is approximately 300 μs and is shown in fig. 10.

Table I summerizes the technical data of the highly

TABLE I. Technical data

Technology	0.4 μm/85 GHz-f_T SiGe bipolar
Level of monolithic integration	VCO with frequency doubler and static frequency divider
Output frequency range	36 GHz - 45.5 GHz
Output power	-12 dBm ... -16 dBm
Phase noise† @ 40 GHz	-79.5 dBc/Hz @ 1 MHz offset
Power consumption	650 mW @ 5 V
PLL settling time	$\leq$ 300 μs
Chip size	0.86 x 0.7 mm^2

† of the free-running VCO with frequency doubler

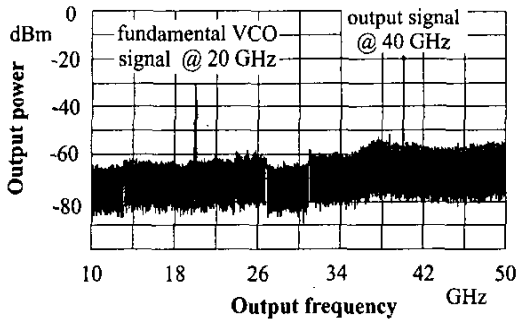

Fig. 9. Spectrum of the output signal at 40 GHz in locked mode (without de-embedding of the losses).

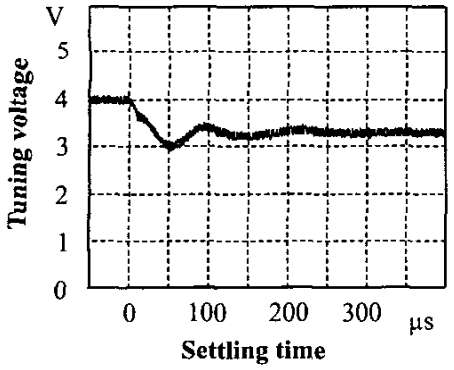

Fig. 10. Settling time of the PLL synthesizer for an output frequency step from 38 GHz to 40 GHz.

integrated phase-locked loop synthesizer.

V. Conclusions

Key building blocks of frequency synthesizers to achieve carrier frequencies beyond 40 GHz are the voltage-controlled oscillator, the frequency divider, and the frequency multiplier. In this paper we demonstrat for the first time the monolithic integration of these three key building blocks on a single chip for output frequencies beyond 40 GHz.

We have achieved a 45 GHz phase-locked loop frequency synthesizer in a pre-production low-cost 0.4 μm/85 GHz-f_T silicon bipolar technology. The synthesizer has a coarse tuning range of 10 GHz. At 40 GHz the output power is -14 dBm. To our knowledge 45 GHz is the highest operating frequency reported for highly-integrated synthesizers up to date.

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